AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1-3. (cancelled)

4. (previously presented) A semiconductor memory, comprising:

a memory cell array constituted by memory cells, each memory cell having a floating electrode, the memory cells being arranged in a matrix on a semiconductor substrate;

a plurality of first trenches formed in said semiconductor substrate, each first trench being formed between said memory cells adjacent to each other along a gate width direction;

a plurality of isolating fillers filled in said first trenches;

a plurality of second trenches formed in said isolating fillers, each said second trench being formed between said floating electrodes of adjacent ones of said memory cells along the gate width direction, and said second trenches being in the shape of an inverted trapezoid; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

5. (previously presented) A semiconductor memory, comprising:

a memory cell array constituted by memory cells, each memory cell having a floating electrode, the memory cells being arranged in a matrix on a semiconductor substrate;

a plurality of first trenches formed in said semiconductor substrate, each first trench being formed between adjacent ones of said memory cells along a gate width direction;

a plurality of isolating fillers filled in said first trenches;

a plurality of second trenches formed in said isolating fillers, each second trench being formed between said floating electrodes of adjacent ones of said memory cells along the gate width direction, and said second trenches being in the shape of a U; and

a word line connected to said memory cells, buried in said second trenches and extending along the gate width direction.

6. (canceled)

7. (currently amended) The semiconductor memory of claim 4, <u>further comprising a gate insulating film in said second trenches,</u> wherein said word line is ~~buried in said second trenches via a~~ <u>on the</u> gate insulating film.

8. (previously presented) The semiconductor memory of claim 7, wherein said gate insulating film includes at least a silicon nitride film.

9. (previously presented) The semiconductor memory of claim 4, wherein a ratio of a top diameter to a bottom diameter of said second trench is greater than a ratio of a top diameter to a bottom diameter of said first trench.

10. (previously presented) The semiconductor memory of claim 4, wherein each of said second trenches is shallower than said first trenches and extends below a surface of said semiconductor substrate.

11. (previously presented) The semiconductor memory of claim 4, wherein said memory is at least one of a NAND and NOR type electrically erasable programmable read only memory.

12-13. (cancelled)

14. (previously presented) A method of manufacturing a semiconductor memory, comprising:

making element isolating regions by forming a plurality of first trenches in a semiconductor substrate, each first trench being made between adjacent ones of memory cell forming regions along a gate width direction;

filling said plurality of first trenches with a plurality of isolating fillers;

making a plurality of floating gate electrodes on said semiconductor substrate at said memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of second trenches in said isolating fillers filled in said first trenches, each second trench being made between adjacent ones of said floating electrodes along the gate width direction, said second trenches being in the shape of an inverted trapezoid; and

forming a word line in said second trenches, said word line extending along the gate width direction.

15. (previously presented) A method of manufacturing a semiconductor memory, comprising:

making element isolating regions by forming a plurality of first trenches in a semiconductor substrate, each first trench being made between adjacent ones of a plurality of memory cell forming regions along a gate width direction;

filling said plurality of first trenches with a plurality of isolating fillers;

making a plurality of floating gate electrodes on said semiconductor substrate at said memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of second trenches in said isolating fillers filled in said first trenches, each second trench being made between adjacent ones of the floating electrodes along the gate width direction, said second trench being in the shape of a U; and

forming a word line in said second trenches, said word line extending along the gate width direction.

16. (previously presented) The method of claim 14, wherein said second trenches are in self-alignment to said floating electrodes.

17. (previously presented) A method of manufacturing a semiconductor memory, the method comprising:

making floating gate electrodes on a semiconductor substrate at memory cell forming regions, said floating gate electrodes having a predetermined gate width;

making a plurality of first trenches in said semiconductor substrate, each said first trench being made between adjacent ones of said floating gate electrodes along a gate width direction, said first trenches being in self-alignment to said floating gate electrodes;

making element isolating regions by filling isolating fillers in said first trenches;

making a side wall spacer on a surface of each of said isolating fillers in a side wall of said floating gate electrodes, said side wall spacer being in self-alignment to said floating gate electrodes;

making a plurality of second trenches in said isolating fillers filled in said first trenches using said side wall spacer as a mask, wherein said second trenches have a narrower width at a bottom thereof than at a top thereof, and a maximum width of said second trenches is smaller than a width of said first trenches; and

forming a word line in said second trenches, said word line extending along the gate width direction.

18. (previously presented) The semiconductor memory of claim 4, wherein each of said second trenches has a second gate insulating film on inner surfaces thereof.

19. (previously presented) The method of claim 14, wherein each of said second trenches has a second gate insulating film on inner surfaces thereof.

20. (previously presented) The method of claim 17, wherein each of said second trenches has a second gate insulating film on inner surfaces thereof.

21. (new) The semiconductor memory of claim 4, wherein each of said second trenches is capable of reducing parasitic capacitance between said floating electrodes of said memory cells adjacent to each other along the gate width direction.

22. (new) The semiconductor memory of claim 5, wherein each of said second trenches is capable of reducing parasitic capacitance between said floating electrodes of said memory cells adjacent to each other along the gate width direction.